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\* Design Summary \*

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Top Level Output File Name : data\_memory.ngc

Primitive and Black Box Usage:

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# BELS : 32

# LUT4 : 32

# FlipFlops/Latches : 32

# FDE : 32

# RAMS : 32

# RAM128X1S : 32

# Clock Buffers : 1

# BUFGP : 1

# IO Buffers : 73

# IBUF : 41

# OBUF : 32

Device utilization summary:

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Selected Device : 6slx9tqg144-3

Slice Logic Utilization:

Number of Slice Registers: 32 out of 11440 0%

Number of Slice LUTs: 96 out of 5720 1%

Number used as Logic: 32 out of 5720 0%

Number used as Memory: 64 out of 1440 4%

Number used as RAM: 64

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 96

Number with an unused Flip Flop: 64 out of 96 66%

Number with an unused LUT: 0 out of 96 0%

Number of fully used LUT-FF pairs: 32 out of 96 33%

Number of unique control sets: 1

IO Utilization:

Number of IOs: 74

Number of bonded IOBs: 74 out of 102 72%

Specific Feature Utilization:

Number of BUFG/BUFGCTRLs: 1 out of 16 6%

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Partition Resource Summary:

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No Partitions were found in this design.

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Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT

GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

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Clock Signal | Clock buffer(FF name) | Load |

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clk | BUFGP | 64 |

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Asynchronous Control Signals Information:

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No asynchronous control signals found in this design

Timing Summary:

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Speed Grade: -3

Minimum period: 1.741ns (Maximum Frequency: 574.432MHz)

Minimum input arrival time before clock: 3.736ns

Maximum output required time after clock: 3.597ns

Maximum combinational path delay: No path found

Timing Details:

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All values displayed in nanoseconds (ns)

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Timing constraint: Default period analysis for Clock 'clk'

Clock period: 1.741ns (frequency: 574.432MHz)

Total number of paths / destination ports: 32 / 32

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Delay: 1.741ns (Levels of Logic = 1)

Source: Mram\_mem1 (RAM)

Destination: readData\_0 (FF)

Source Clock: clk rising

Destination Clock: clk rising

Data Path: Mram\_mem1 to readData\_0

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

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RAM128X1S:WCLK->O 1 0.854 0.580 Mram\_mem1 (address[6]\_read\_port\_3\_OUT<0>)

LUT4:I3->O 1 0.205 0.000 Mmux\_readData[31]\_writeData[31]\_mux\_6\_OUT11 (readData[31]\_writeData[31]\_mux\_6\_OUT<0>)

FDE:D 0.102 readData\_0

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Total 1.741ns (1.161ns logic, 0.580ns route)

(66.7% logic, 33.3% route)

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Timing constraint: Default OFFSET IN BEFORE for Clock 'clk'

Total number of paths / destination ports: 640 / 352

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Offset: 3.736ns (Levels of Logic = 3)

Source: address<0> (PAD)

Destination: readData\_0 (FF)

Destination Clock: clk rising

Data Path: address<0> to readData\_0

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

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IBUF:I->O 32 1.222 1.291 address\_0\_IBUF (address\_0\_IBUF)

RAM128X1S:A0->O 1 0.336 0.580 Mram\_mem2 (address[6]\_read\_port\_3\_OUT<1>)

LUT4:I3->O 1 0.205 0.000 Mmux\_readData[31]\_writeData[31]\_mux\_6\_OUT121 (readData[31]\_writeData[31]\_mux\_6\_OUT<1>)

FDE:D 0.102 readData\_1

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Total 3.736ns (1.865ns logic, 1.871ns route)

(49.9% logic, 50.1% route)

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Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'

Total number of paths / destination ports: 32 / 32

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Offset: 3.597ns (Levels of Logic = 1)

Source: readData\_31 (FF)

Destination: readData<31> (PAD)

Source Clock: clk rising

Data Path: readData\_31 to readData<31>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

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FDE:C->Q 1 0.447 0.579 readData\_31 (readData\_31)

OBUF:I->O 2.571 readData\_31\_OBUF (readData<31>)

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Total 3.597ns (3.018ns logic, 0.579ns route)

(83.9% logic, 16.1% route)

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Cross Clock Domains Report:

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Clock to Setup on destination clock clk

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| Src:Rise| Src:Fall| Src:Rise| Src:Fall|

Source Clock |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|

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clk | 1.741| | | |

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Total REAL time to Xst completion: 10.00 secs

Total CPU time to Xst completion: 10.38 secs

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Total memory usage is 4506632 kilobytes

Number of errors : 0 ( 0 filtered)

Number of warnings : 0 ( 0 filtered)

Number of infos : 1 ( 0 filtered)